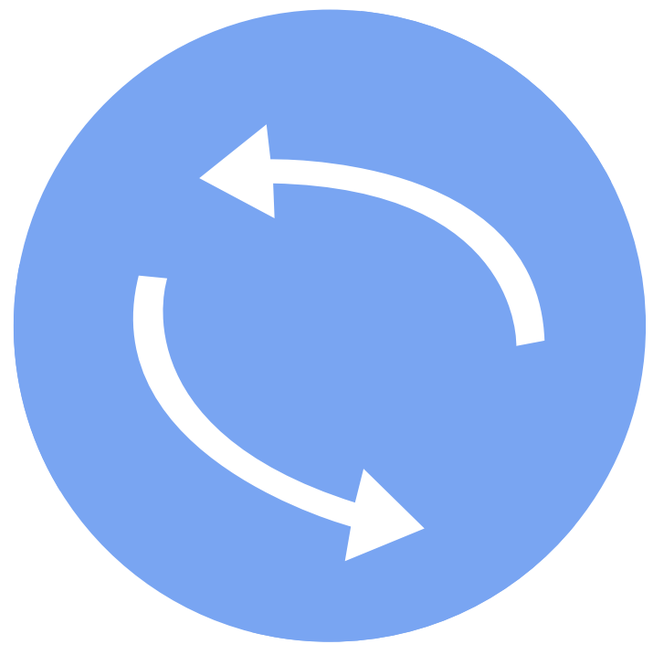
IGNOU

MCS-202

30 MOST REPEATED QUESTIONS



Curated List of 30 Questions that are seen to be repeated frequently in the examinations.

By **FarLearner.com**

MCS-202 Most Repeated Questions

1 . Perform the following operations using signed 2's complement notation of 8 bits (including sign bit). Also indicate overflow, if any.

Found in Dec 2021 (1 a) , Dec 2022 (1 a) , Dec 2023 (1 a) , June 2023 (1 a)

(i) Add −28 and +127

Step 1: Convert to 8-bit binary

+127 = 01111111

28 in binary = 00011100

−28 → Take 2's complement

Invert → 11100011

Add 1 → 11100100

So,

−28 = 11100100

Now add:

11100100

+ 01111111

---

1 01100011

Ignore carry out.

Result = 01100011

01100011 = +99

Actual decimal result: −28 + 127 = 99

Since result is within range and sign is correct → No overflow

(ii) Subtract −56 from −77

−77 − (−56)

= −77 + 56

= −21

Now verify using binary:

77 = 01001101

−77 →

Invert → 10110010

Add 1 → 10110011

56 = 00111000

Add:

10110011

+ 00111000

11101011

11101011 is negative.

Take 2’s complement:

Invert → 00010100

Add 1 → 00010101 = 21

So result = −21

Within range → No overflow

(iii) Add +28 and +100

28 = 00011100

100 = 01100100

Add:

00011100

+ 01100100

10000000

10000000 represents −128

Actual decimal result: 28 + 100 = 128

But 128 is outside +127 limit.

Two positive numbers gave negative result → Overflow occurs

FarLearner.com

2 . Simplify the following function using Karnaugh's map (K-map) and draw the logic circuit of the function so obtained.

Found in Dec 2021 (1 b) , Dec 2022 (2 b) , Dec 2023 (1 b) , Dec 2024 (2 a) , June 2022 (1 b) , June 2023 (1 b) , June 2024 (2 a)

$F(A, B, C, D) = \Sigma (0, 3, 5, 7, 9, 10, 11, 12, 15)$

After grouping adjacent minterms in K-map, simplified expression is:

$F = A'C'D' + B'D + AC + A'BD$

Logic Circuit

- Use NOT gates to generate A', B', C', D'
- Use AND gates to generate each product term
- Use OR gate to combine outputs

Structure:

- AND1 → A'C'D'
- AND2 → B'D
- AND3 → AC
- AND4 → A'BD
- All outputs connected to OR gate

MCS-202 Most Repeated Questions

3 . Differentiate between Von Neumann and Harvard architecture.

Found in Dec 2021 (2 d) , Dec 2022 (2 a) , Dec 2023 (2 a) , June 2024 (1 a)

Answer : Von Neumann Architecture

- Uses single memory for both data and instructions.
- Uses one common bus for transferring data and instructions.
- Cannot access data and instruction at the same time.
- Slower due to Von Neumann bottleneck.
- Simpler design and easier to implement.
- Less expensive compared to Harvard architecture.
- Commonly used in general-purpose computer systems.

Harvard Architecture

- Uses separate memories for data and instructions.
- Uses separate buses for data and instructions.
- Can access data and instructions simultaneously.
- Faster performance because there is no bottleneck.
- More complex design.
- More
- Co signal proc

4 . What is the importance of DMA? Explain its functioning.

Found in Dec 2021 (1 d) , Dec 2023 (3 c) , Dec 2024 (1 f)

DMA (Direct Memory Access) is a technique that allows an I/O device to transfer data directly to or from main memory without continuous involvement of the CPU. A special hardware unit called the DMA controller manages this transfer.

Importance of DMA

- Reduces CPU Overhead

The CPU is free to perform other tasks while data transfer takes place.

- faster Data Transfer

High-speed devices (like disk drives) can transfer large blocks of data efficiently.

- Improved System Performance

Parallel operation of CPU and I/O improves overall throughput.

- Efficient Block Transfer

Suitable for transferring large data blocks instead of byte-by-byte

MCS-202 Most Repeated Questions

Modes of DMA Transfer

- Burst Mode – Entire block transferred at once.
- Cycle Stealing Mode – Transfers one word at a time.
- Transparent Mode – Transfers when CPU is idle.

5 . Explain the working of a micro-programmed control unit with the help of a diagram.

Found in Dec 2021 (1 f) , Dec 2023 (4 d) , Dec 2024 (4 b)

A micro-programmed control unit is a type of control unit in which control signals are generated by microinstructions stored in control memory instead of using hardwired logic circuits.

It was introduced by Maurice Wilkes.

In this system, each machine instruction is executed by a sequence of microinstructions.

Basic Components

A micro-programmed control unit consists of:

- Control Memory (ROM or Writable Control Store)
- Con
- Co
- Micr

Control signal generation logic

6 . List the features or advantages of RISC architecture.

Found in Dec 2021 (4 b) , Dec 2022 (4 c) , Dec 2023 (4 c)

RISC (Reduced Instruction Set Computer) architecture has the following advantages:

- Simple and small instruction set.
- Faster execution of instructions.
- Fixed-length instructions.
- Easy instruction pipelining.
- Reduced hardware complexity.
- Better performance due to load/store architecture.

Use of Large Register File in RISC

RISC architectures use a large number of general-purpose registers.

Uses:

- Reduces memory access since operands are stored in registers.
- Improves execution speed.
- Supports efficient pipelining.
- Helps in passing parameters between functions.

7 . Explain the use of a large register file in the context of RISC architecture.

Found in Dec 2021 (4 b) , Dec 2024 (1 e) , June 2022 (4 d)

RISC (Reduced Instruction Set Computer) architecture has the following advantages:

- Simple and small instruction set.
- Faster execution of instructions.
- Fixed-length instructions.
- Easy instruction pipelining.
- Reduced hardware complexity.
- Better performance due to load/store architecture.

Use of Large Register File in RISC

RISC architectures use a large number of general-purpose registers.

Uses:

- Reduces memory access since operands are stored in registers.
- Improves execution speed.
- Supports efficient pipelining.
- Hel s.

MCS-202 Most Repeated Questions

8 . Explain instruction pipelining with the help of a diagram.

Found in Dec 2021 (5 b i) , Dec 2023 (1 f) , Dec 2024 (5 b i)

Instruction pipelining is a technique in which multiple instruction phases are executed simultaneously by dividing instruction execution into stages.

Typical stages:

- Fetch
- Decode
- Execute

Diagram

Instruction 1 : Fetch Decode Execute

Instruction 2 : Fetch Decode Execute

Instruction 3 : Fetch Decode Execute

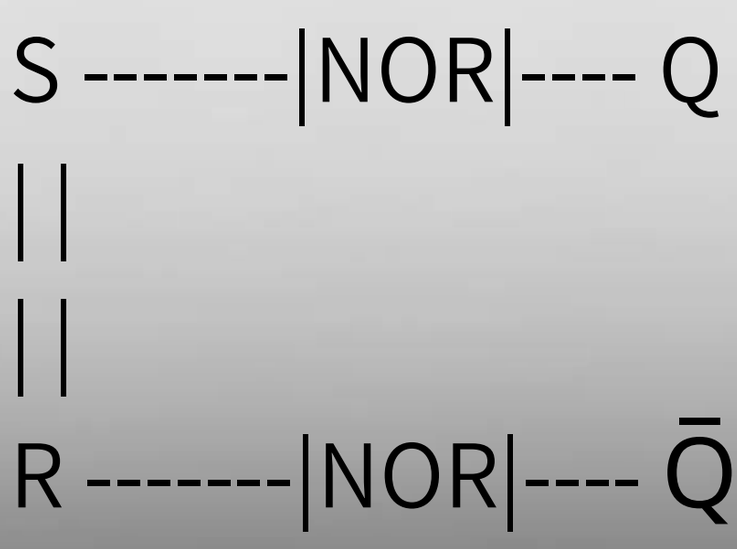
Thus, while one instruction is being executed, another is being decoded and a third is being fetched. This increases CPU throughput.

MCS-202 Most Repeated Questions

9 . Draw the block diagram and characteristic table of an S-R flip-flop.

Found in Dec 2021 (2 b) , June 2022 (2 d) , June 2024 (2 c)

Block Diagram (Using NOR Gates)



Working

- S = 1, R = 0 → Set (Q = 1)
- S = 0, R = 1 → Reset (Q = 0)
- S = 0, R = 0 → No change
- S = 1, R = 1 → Invalid condition

Characteristic Table

S R → Next State Q_{n+1}

0 0 → Q_n

0 1 → 0

1 0 → 1

1 1 → Invalid

Excitation Table

Present → Next → Required Inputs

0 → 0 → S=0, R=X

0 → 1 → S=1, R=0

1 → 0 → S=0, R=1

1 → 1 → S=X, R=0

(X = Don’t care)

10 . Explain the concept of memory hierarchy with the help of a diagram.

Found in Dec 2021 (3 a) , June 2022 (3 b)

Why Memory Hierarchy is Needed

Memory hierarchy is created to achieve:

- High speed
- Large storage capacity
- Low cost per bit

No single memory type satisfies all three requirements.

- Cache → Very fast but expensive and small
- RAM → Moderate speed and cost
- Har

Hence, a cost, and capacity.